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Attorneys for Defendant and Counterclaimant
FAIRCHILD SEMICONDUCTOR CORPORATION

UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation; and ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
(Consolidated with Case No. C 07-2664 JSW)

DECLARATION OF DR. RICHARD A. BLANCHARD IN SUPPORT OF FAIRCHILD'S MOTION TO COMPEL PRODUCTION OF DOCUMENTS

Date: September 16, 2008
Time: 9:00 a.m.
Courtroom: Courtroom E, 15th Floor

Hon. Elizabeth D. Laporte

I, Dr. Richard A. Blanchard, declare as follows:

Biography

1. I have been retained as an expert regarding semiconductor technology by Defendant and Counterclaimant Fairchild Semiconductor Corporation ("Fairchild"). This Declaration is submitted in support of Fairchild's Motion to Compel Production of Documents ("Motion to Compel"). I have personal knowledge of the matters stated herein and if called to testify as a witness, I could and would competently testify thereto.

2. I received a BSEE degree in 1968 and an MSEE degree in 1970 from MIT, and a PhD in Electrical Engineering from Stanford University in 1982. I was an Associate Professor, Assistant Division Chairman of the Engineering & Technology Division at Foothill College from 1974 to 1978, where among other things, I developed the curriculum for the Semiconductor Technology Program.

3. I have over 35 years of experience in the semiconductor and electronics industries. I am an exclusive expert at the Silicon Valley Expert Witness Group, Inc. ("SVEWG") and have extensive consulting experience since 1998 for SVEGW. Prior to working for SVEWG, I was Principal Engineer and Division Manager of the Electrical/Electronic Division of Failure Analysis (Exponent) Associates, Inc., from 1991 to 1998. As Division Manager, my duties included failure analysis and reverse engineering of solid-state electronic components and circuits, failure analysis of electric and electronic systems, subsystems, and components, and consulting with respect to Power MOS and Smart Power Technologies. Prior to that, I was employed by IXYS Corporation from 1987-1991, by Siliconix, Inc., from 1982-1987, by Supertex, Inc., from 1976-1982, by Cognition, Inc., from 1976 to 1978, by Foothill College from 1974-1978, as an independent consultant to the semiconductor industry from 1974-1976 and by Fairchild Semiconductor from 1970-1974.

4. I have testified in court and in deposition on numerous occasions as an expert witness, and I have served as a court-appointed special master. I have published several books and numerous articles on semiconductor design and process development, as well as failure analysis. I hold more than 130 U.S. patents on semiconductor technology. I am a member of the IEEE, the Electrostatic Discharge Society, and the International Microcircuits and Packaging Society, and the Electron Device Failure Analysis Society (EDFAS).

Fairchild Mo Patents

5. I am familiar with the Fairchild Mo patents, and have reviewed their specifications and claims.[1] The Fairchild Mo Patents relate to trench power MOSFETs. A power MOSFET device with a trench gate design includes one or more gates formed in trenches that are etched vertically into an underlying material. When a trench device is turned on by applying a voltage to the gate, current flows vertically through the channel that is formed adjacent to the vertical sides of the gate. A representative embodiment from the patents is set forth below:

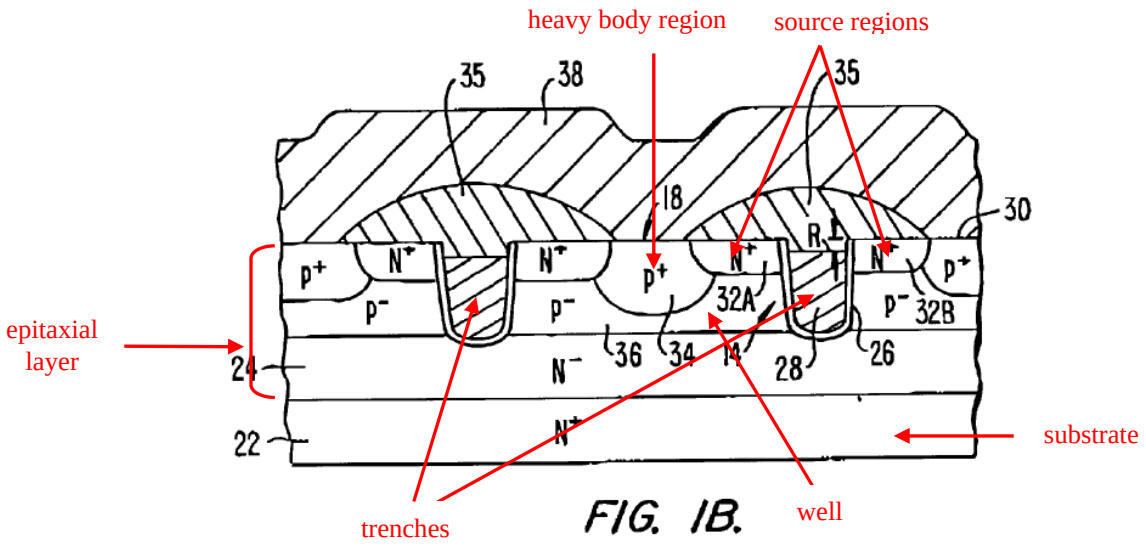

FIG. 1B.

('481 patent, Fig. 1B (annotated).) As shown in this drawing, the power MOSFET includes a substrate on which an epitaxial layer is formed. It further includes a doped well formed in the epitaxial layer, and a more heavily doped heavy body region formed in the well. Additionally, the power MOSFET includes trenches lined with a gate oxide layer and then filled with a conductive material (usually polysilicon) which form gate electrodes. Source regions are formed on each side of each trench.

6. The Fairchild Mo Patents claim a novel way of controlling the phenomenon of breakdown in the active area of power MOSFETs. Breakdown is an unwanted effect where current flows between the source and the drain even if no voltage is applied to the gate, i.e., the device is "on"

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[1] In this declaration, the term "Fairchild Mo patents" refers to U.S. Patent Nos. 6,429,481 ("the '481 patent"), 6,521,497 ("the '497 patent"), 6,710,406 ("the '406 patent"), 6,828,195 ("the '195 patent"), and 7,148,111 ("the '111 patent").

when it should be "off." Generally, current can only flow easily in one direction across a P-N junction formed in a semiconductor device. This occurs when the P-N junction has voltage applied across it in the forward direction. If, however, the polarity of the voltage is reversed across the junction, current will not flow unless the voltage is increased to the point that current carriers are actually ripped from their locations in the silicon. This generally unwanted effect is named "avalanche breakdown." The reverse voltage at which a power MOSFET will experience avalanche breakdown is referred to as its "breakdown voltage."

7. Power MOSFET designers go to great lengths to control breakdown because it can irreversibly damage the device. The Fairchild Mo Patents address the important goal of avoiding having the device go into breakdown near the fragile gate structure formed in the trenches. If breakdown occurs near the gate, the thin gate oxide surrounding the gate electrode in the trench can be damaged. The Fairchild Mo Patents claim a novel method and design for forming a heavy body region in the well which serves to insure that breakdown current is spaced away from the trenches. If the breakdown current is spaced away from the trenches, the device will have a much better chance of surviving the breakdown event, a characteristic that is referred to as "ruggedness." By enhancing power MOSFET ruggedness, the Fairchild Mo Patents achieve an important goal of power MOSFET design.

8. Each claim of the Fairchild Mo patents relates to the structure, operation, and/or manufacturing of power MOSFET devices.

9. **Manufacturing:** Some claims relate to methods of making power MOSFET devices. The '195 patent, for example, claims a method of manufacturing a trench power MOSFET device, and includes the steps of "providing a semiconductor substrate," "forming a plurality of trenches," "forming a doped well," and "forming a heavy body." ('195 patent, claim 1). Similarly, claim 1 of the '497 patent relates to a method of manufacturing power MOSFET devices and includes the steps of "implanting a first dopant at a first energy level and dosage into the substrate, to form a doped well," implanting "a second dopant at a second energy and dosage to form a first doped portion of a heavy body," and implanting "a third dopant at a third energy and dosage to form a second doped portion of the heavy body." ('497 patent, claim 1). Other claims of the Fairchild Mo patents also relate to

manufacturing methods. (e.g., '195 patent, claims 2, 6-13, 21-22; '497 patent, claims 2-7, 11-13, 15-17; '111 patent, claims 29-35).

10. **Device Structure and Operation:** In addition to manufacturing, claims of the Fairchild Mo patents relate to the structure and operation of power MOSFET devices. The '481 patent, for example, claims a trench power MOSFET device that has the structural features of having "a semiconductor substrate," "a trench extending a predetermined depth into said semiconductor substrate," "a doped well," and "a doped heavy body." ('481 patent, claim 1). Additionally, this claim includes operational limitations requiring that the "transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor." (*Id.*). Other claims of the Fairchild Mo patents similarly include both structural and operational limitations. (e.g., '406 patent, claim 1). Additionally, some of the Fairchild Mo patents include method claims that have operational limitations. Claim 29 of the '111 patent, for example, claims a method requiring, among other things, the step of "adjusting a dopant profile of the plurality of heavy body regions so that peak electric field is moved away from a nearby trench" which results in "avalanche current that is substantially uniformly distributed." ('111 patent, claim 29). This claim therefore relates in part to the way in which the power MOSFET device operates during certain circumstances. Other method claims of the Fairchild Mo patents similarly include limitations relating to the operation of a device. (e.g., '195 patent, claim 22 ("adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor")).

Manufacturing Documents

11. In my 35 years of experience in the semiconductor and electronics industry, I have become familiar with the types of documents that are typically prepared and maintained by semiconductor companies relating to the manufacture of their devices.

12. Manufacturing documents describe in detail the method by which a semiconductor device is manufactured. These manufacturing documents include recipes, process flows, GDS files, wafer specifications, epitaxial layer specifications, and other documents needed to manufacture a semiconductor device. Recipes are important manufacturing documents as they contain parameters for each semiconductor manufacturing step and may include information such as temperature, time,

gas flows, and other parameters used for a particular manufacturing step. For an implant step, for example, the recipe may describe the implant dopant type, implant dosage, and energy level for the implant step. Process flows describe the sequence of steps of the manufacturing process, including the order of deposition, etch, and implants steps used in the manufacture of devices. GDS files specify the shape and location of clear and opaque regions on the masks used during photolithographic steps of the manufacturing sequence to manufacture various layers of the device. Semiconductor manufacturers typically use technology files or bias tables in connection with GDS files, which correlate each process layer of the device with GDS layer information. Wafer and epitaxial layer specifications describe the parameters and properties of the starting wafers used in the manufacture of a semiconductor device.

13. In my experience in the semiconductor industry, the manufacturing documents described above are standard documents used in the manufacture of semiconductor devices, including power MOSFET devices. A person skilled in the art can use the above manufacturing documents to understand how a device is made. These documents can therefore assist in evaluating whether the manufacturing methods claimed in the Fairchild Mo patents are used during the manufacture of AOS's products.

14. Additionally, given that the manufacturing documents described above provide details concerning how devices are made, they can be used to evaluate the characteristics of the structures in a finished device. They can also be used to develop simulations of the structural and electrical properties of the devices. As explained below, the development of simulations require input information concerning how the devices are made, including information concerning specific steps in the manufacturing process. Such information is typically found in recipes. Accordingly, recipes can be highly relevant to the simulation of power MOSFET devices.

Simulation Documents

15. I am familiar with the types of simulations that are typically performed in designing semiconductor devices, including power MOSFET devices, and am familiar with the categories of documents and information that are typically used and created in connection with such simulations.

16. In my experience, simulations are often used during the design and development of

semiconductor devices, including power MOSFET devices. Simulations involve using computer software to model the structure and electrical behavior of devices. There are several types of simulations. One type, known as process simulation, involves modeling the structure of a device. Another type, known as device simulation, involves modeling the electrical behavior of a device during its operation.

17. To perform simulations, one must input certain information into the simulation program describing the device structure and how the device is manufactured. Such input information is typically found in files referred to as coefficient files, input command files, mask files, structure boundary files, and measured doping files.

18. Using the input information concerning a device, a simulation program develops a simulation of the structural and operational features of a device. The output of the simulation may be in the form of simulated electrical data, output files (structure, doping, and/or grid output files), or other information. The output data may also include drawings of the device structure showing current paths, electric field lines, or other information.

19. Given that simulations can be used to simulate (i.e., model or predict) the structure and operation of devices, they can therefore assist in evaluating whether the structural and operational features claimed in the Fairchild Mo patents are present in AOS's products.

Device Structure Documents

20. I am familiar with techniques commonly used in the semiconductor industry for analyzing the structural features of semiconductor devices.

21. One technique commonly used to analyze semiconductor devices is secondary ion mass spectrometry ("SIMS"). SIMS is a technique for the characterization of solid surfaces and thin films. SIMS is often used to obtain a doping profile showing the concentration of a dopant as a function of the depth of implantation into the silicon of different dopants, such as phosphorus, boron and arsenic, that may be present in a cross-section of a semiconductor device. Fairchild cited SIMS data as evidence of infringement in its preliminary infringement contentions for the Fairchild Mo patents. (e.g., Fairchild's Preliminary Infringement Contentions, dated August 31, 2007, Fig. AO4410-5).

22. Another technique commonly used to analyze semiconductor devices is Scanning

Capacitance Microscopy ("SCM"). SCM can be used to determine the dopant profile at the exposed surface of a device being analyzed. SCM is often used to obtain information regarding the conductivity type (n-type or p-type) and the range of relative doping concentration at lateral and vertical distances throughout a substrate of a cross-section of a semiconductor device. SCM gives two-dimensional information regarding the dopant profile. Fairchild cited SCM images as evidence of infringement in its preliminary infringement contentions for the Fairchild Mo patents. (e.g., Fairchild's Preliminary Infringement Contentions, dated August 31, 2007, Fig. AO4410-4).

23. Another technique commonly used to analyze semiconductor devices is Spreading Resistance Profiling ("SRP"). SRP techniques can be used to determine the dopant profile at the exposed surface of a device being analyzed. SRP is often used to obtain information regarding the range of relative doping concentration at vertical distances across a region of a semiconductor device. SRP gives one-dimensional information regarding the dopant profile.

24. Another technique commonly used to analyze semiconductor devices is Scanning Electron Microscopy ("SEM"). SEM is a technique for high-resolution imaging of surfaces. SEM is often used to determine structures by cross-sectioning the device and then using a staining technique. Other techniques such as SIMS and SCM are often then used to obtain further information with respect to the structures in the device. Fairchild cited SEM images as evidence of infringement in its preliminary infringement contentions for the Fairchild Mo patents. (e.g., Fairchild's Preliminary Infringement Contentions, dated August 31, 2007, Fig. AO4410-3).

25. In the semiconductor field, "in-line data" refers to quality assurance data typically measured by a semiconductor manufacturer at various points during the manufacturing process to verify that a given lot of devices has been properly manufactured up to that point in the manufacturing process. In-line data can establish the structural features of the device (e.g., trench depth) at various points in the manufacturing process, and is therefore useful in evaluating the features of a finished device.

26. Documents that reflect the results of each of the techniques described above may show the structural features of AOS's devices (including the shape and location of various regions in the device, as well as the conductivity type and dopant concentration of such regions). Manufacturing

documents can therefore assist in evaluating whether the structural features claimed in the Fairchild Mo patents are present in AOS's products.

Device Operation Documents

27. I am very familiar with techniques commonly used in the semiconductor industry for evaluating the operational characteristics of semiconductor devices. For power MOSFET devices, the data used for such evaluations include "electrical breakdown current-voltage characteristics data," "operational transistor current-voltage characteristics data," and "unclamped inductive switching data."

28. The term "electrical breakdown current-voltage characteristics data" refers to the measured current-voltage characteristics that are obtained when increasing voltage is applied to a semiconductor device causing a large increase in current flow. Data of this type contains information regarding the breakdown characteristics of a device.

29. The term "operational transistor current-voltage characteristics data" refers to the raw data underlying standard current-voltage graphs published in typical product datasheets by semiconductor manufacturers that shows the relationship between voltage and current at various points in a device.

30. The term "unclamped inductive switching data" refers to data directed to understanding how a device will react to a sudden significant increase in voltage which may cause a large current flow in the device. This data can be used to evaluate the location of breakdown in a device.

31. Semiconductor manufacturers often publish datasheets for their devices that contain charts, graphs and plots that provide information about the operating characteristics and performance of the devices. (e.g., Datasheet for AOS's AO4410). The graphs, charts and plots in a datasheet are typically created using raw data obtained by the manufacturer from one or more of the devices about which the datasheet provides information. This data can be used to understand the structure and operation of devices, including their breakdown characteristics.

32. The categories of documents described above, in combination with information concerning device structure, can be used to evaluate the operational features of semiconductor devices, including the characteristics of avalanche breakdown and avalanche current in the devices.

This information therefore can assist a person skilled in the art in evaluating whether the operational features claimed in the Fairchild Mo patents are present in AOS's products.

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I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct to the best of my knowledge and belief.

Executed this 12th day of August, 2008, in Mountain View, California.

Richard A. Blanchard

Richard A. Blanchard, Ph. D.

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